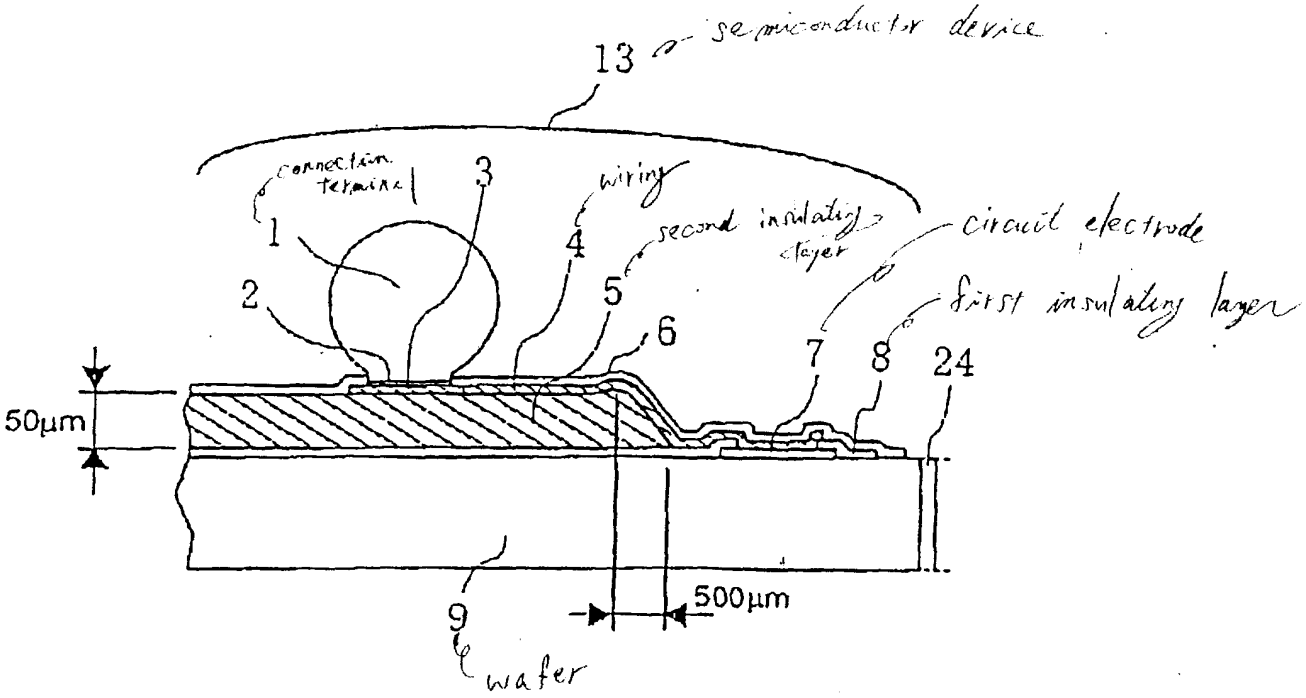

Fig. 1 Semiconductor device
(in the independent claim 39 etc.)

SKETCH A

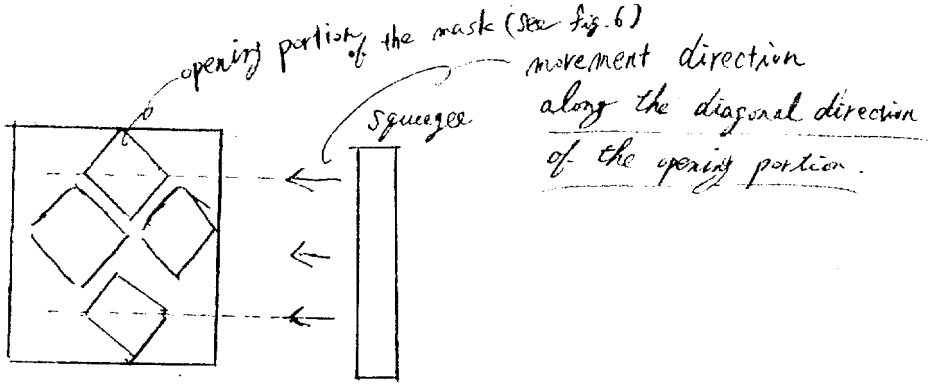

Fig. forming of insulating layer by mask-printing (in the Claims 50 and 62)
(see the figs. 6 and 7)

SKETCH B

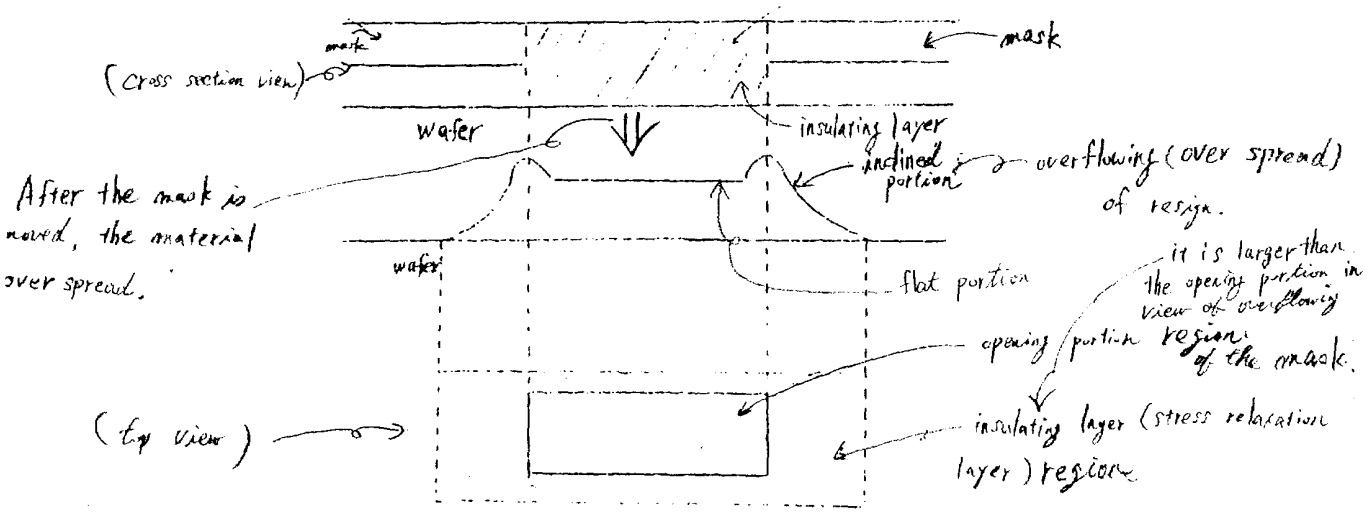

Fig. forming of a stress relaxation layer (in the claim 52 and 64

SKETCH C

FIG. 4

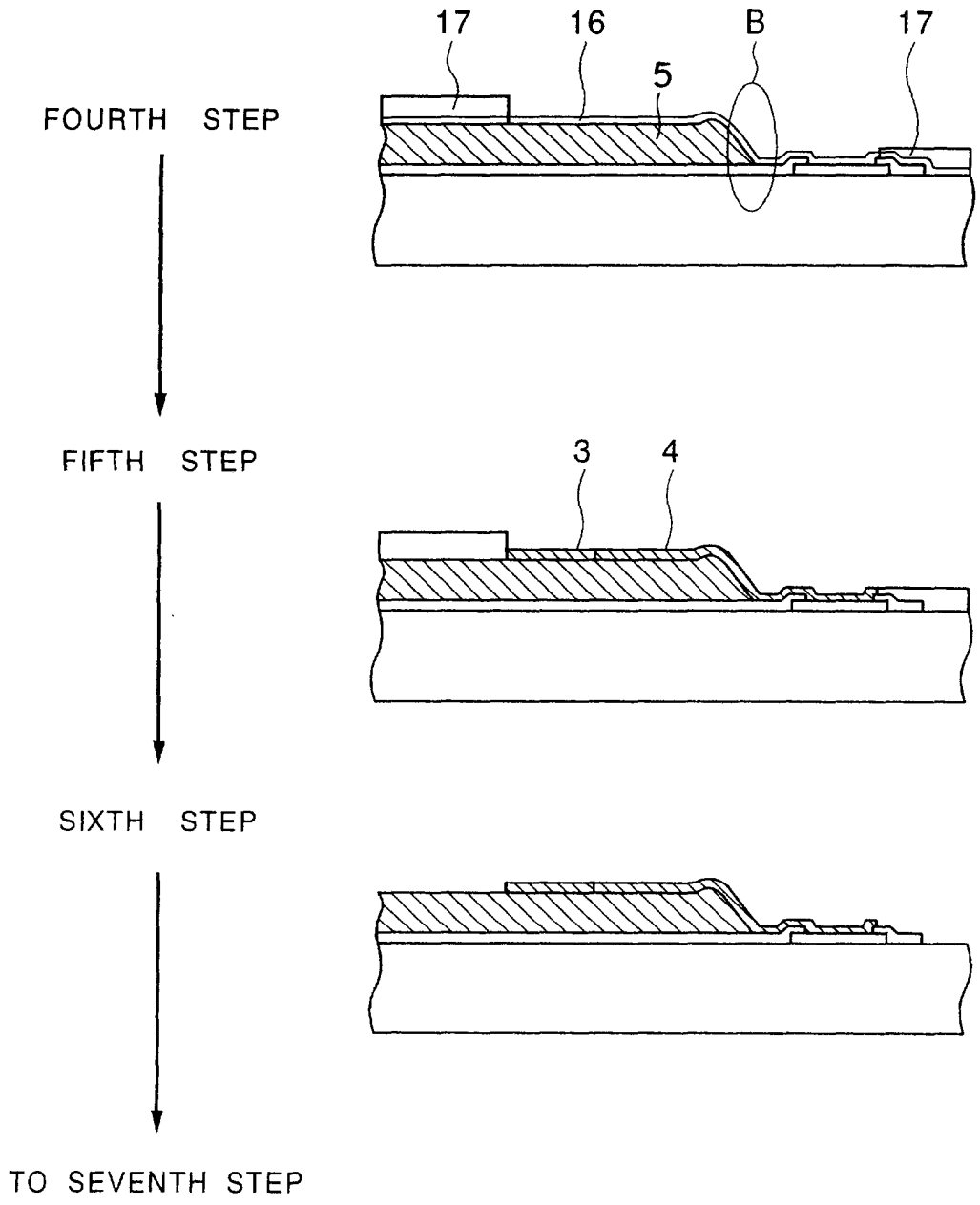
17
16
B
17
5
FOURTH STEP
FIFTH STEP
3
4
SIXTH STEP
TO SEVENTH STEP

FIG. 31
(PRIOR ART)

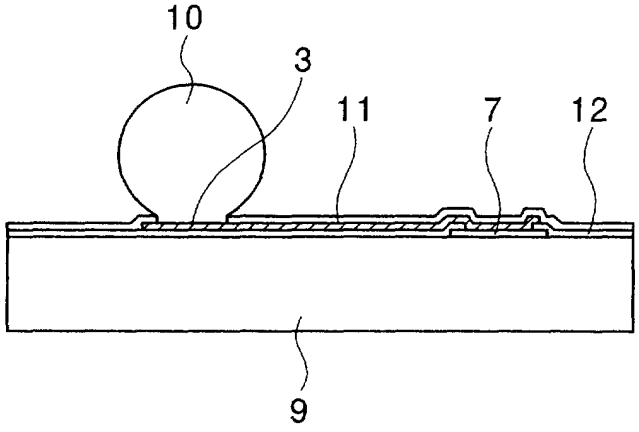

FIG. 32
(PRIOR ART)